CLAIM(S)

What is claimed is:

1. A data communication method comprising the steps of:

a. receiving elements of a first data sequence (Tx,a) at a first rate controlled by a first clock signal (CLK3L) and processing the first data sequence to generate elements of a second data sequence (T3x,a) at a second rate controlled by a second clock signal (CLK1L), wherein the second rate is higher than the first rate and wherein the second data sequence is an encoded version of the first data sequence;

b. encoding the second data sequence into an analog signal (A1) and transmitting the analog signal via a communication channel;

c. receiving and processing the analog signal transmitted by the communication channel to generate elements of a third data sequence (R3x,a) at a third rate controlled by a third clock signal (CLK1R); and

d. processing the third data sequence (R3x,a) to generate elements of a fourth data sequence (Rx,a) at a fourth rate controlled by a fourth clock signal (CLK3R), wherein the fourth rate is lower than the third rate, and wherein the first and fourth data sequences are substantially similar and forwarding the fourth data sequence at the fourth rate.

2. The method in accordance with claim 1 wherein the second and third clock signals are independently generated and are non-coherent.

3. The method in accordance with claim 2 further comprising the steps of:

e. deriving the first clock signal from the second clock signal, and

f. deriving the fourth clock signal from the third clock signal.

4. The method in accordance with claim 3 wherein step e comprises the substeps of:

e1. generating a plurality of reference clock signals, each having edges occurring with a frequency matching a frequency the second clock signal but with a unique phase; and

e2. generating edges of the second clock signal in response to edges of the reference clock signals selected such that the first clock signal has a time-average frequency substantially matching a frequency of the fourth clock signal.

5. The method in accordance with claim 3 wherein step f comprises the substeps of:

f1. generating a plurality of reference clock signals, each having edges occurring with a frequency matching a frequency the third clock signal but with a unique phase; and

f2. generating edges of the fourth clock signal in response to edges of the reference clock signals selected such that the fourth clock signal has an time-average frequency substantially matching that of the first clock signal.

6. The method in accordance with claim 3

wherein step a comprises the substeps of:

a1. masking portions of the second clock signal (CLK1L) to produce a fifth clock signal (CLK2L), and

a2. shifting elements of the first data sequence (Tx,a) into a first-in,first-out (FIFO) buffer at the first rate controlled by the first clock signal (CLK3L);

a3. shifting elements of the first data sequence out of the first FIFO buffer at a fifth rate controlled by the fifth clock signal (CLK2L);

a4. processing the first data sequence as it is shifted out of the first FIFO buffer to generate the elements of the second data sequence (T3x,a) at the second rate controlled by the second clock signal (CLK1L), and

wherein step d comprises the substeps of:

d1. masking portions of the third clock signal (CLK1R) to produce a sixth clock signal (CLK2R),

d2. processing the third data sequence (R3,xa) to generate elements of the fourth data sequence (R1,a) at a sixth rate controlled by the sixth clock signal (CLK2R),

d3. shifting elements of the fourth data sequence into a second FIFO buffer at a sixth rate controlled by the sixth clock signal (CLK2R), and

d4. shifting elements of the fourth data sequence out of the second FIFO buffer and forwarding them at the fourth rate controlled by the fourth clock signal (CLK3R).

7. The method in accordance with claim 6

wherein substep a4 comprises the substeps of:

a41. trellis code modulation encoding the first data sequence as it is shifted out of the FIFO buffer to generate elements of a fifth data sequence (T2x,a), and

a42. applying the fifth data sequence as input to a first filter clocked which interpolates elements of the fifth data sequence (T2x,a) to produce elements of the second data sequence (T3x,a) at said second rate, and

wherein substep d2 comprises the substeps of:

d21. applying the third data sequence as input to a second filter which interpolates elements of the third data sequence (T2x,a) to produce elements of a sixth data sequence (R3x,a) at said third rate, and

d22. trellis code modulation encoding the sixth data sequence to generate elements of the fourth data sequence (R1x,a) at the sixth rate.

8. The method in accordance with claim 7

wherein the first filter is a finite impulse response (FIR) filter producing each element of the second data sequence as a weighted sum of a plurality of elements of the fifth data sequence with weighting controlled by values of first coefficients applied as input to the first filter, and

wherein the second filter is a finite impulse response filter producing each element of the seventh data sequence as

a weighted sum of a plurality of elements of the third data sequence with weighting controlled by values of second coefficients applied as input to the second filter.

9. The method in accordance with claim 8 further comprising the steps of:

g. periodically adjusting values of the first coefficients supplied as input to the first filter in response to the second clock signal, and

h. periodically adjusting values of the second coefficients supplied as input to the second filter in response to the third clock signal.

10. The method in accordance with claim 9 wherein values of the second coefficients are adjusted in response to the sixth data sequence.

11. A transceiver comprising:

a source of a first clock signal having edges that are periodic with a first frequency;

first means for masking a portion of the edges of the first clock signal to produce a second clock signal (CLK2R) and for generating a periodic third clock signal of a second frequency lower than the first frequency, wherein the second frequency is substantially equal to a time-average frequency of occurrence of edges of the second clock signal;

second means for receiving and storing elements of a first data sequence (Tx,a) at a rate controlled by the third clock signal (CLK3L) and for reading out elements of the first data sequence at a rate controlled by the second clock signal;

third means for processing the first data sequence read out of the third means to generate elements of a second data sequence (T3x,a) at a rate controlled by a first clock signal (CLK1L), wherein the second data sequence is an encoded version of the first data sequence;

fourth means for generating a first analog signal (A1) having successive magnitudes controlled by the second data sequence;

fifth means for receiving and processing a second analog signal having successive magnitudes representing a third data sequence to generate elements of a fourth data sequence (R3x,a) at a rate controlled by the first clock signal (CLK1L);

sixth means for processing the fourth data sequence (R3x,a) to generate elements of a fifth data sequence (R1x,a) at a rate controlled by the second clock signal (CLK3L); and

seventh means for receiving and storing elements of the fifth data sequence at a rate controlled by the second clock signal and for reading out elements of the fifth data sequence at a rate controlled by the third clock signal.

12. The transceiver in accordance with claim 11 wherein the third means comprises:

eighth means (79) for encoding the first data sequence read out of the third means to generate elements of a sixth data sequence (T2,xa); and

ninth means (80) for interpolating elements of the sixth data sequence (T2x,a) to produce elements of the second data sequence (T3x,a) at said second rate.

13. The transceiver in accordance with claim 12 wherein the sixth means comprises:

tenth means (93) for interpolating elements of the fourth data sequence (R3x,a) to generate elements of a seventh data sequence (R2x,a) at a rate controlled by the first clock signal (CLK1L); and

eleventh means (94) for decoding elements of the seventh data sequence to generate elements of the fifth data sequence at a rate controlled by the second clock signal.

14. The transceiver in accordance with claim 13 wherein the first means adjusts the second frequency of the third

clock signal and the time-average frequency of the second clock signal in response to the seventh data sequence.

15. The transceiver in occurrence with claim 13

wherein the ninth means comprises a first finite impulse response (FIR) filter producing each element of the second data sequence as a weighted sum of a plurality of elements of the sixth data sequence with weighting controlled by values of first coefficients applied as input to the first filter, and

wherein the tenth means comprises a second FIR filter producing each element of the fifth data sequence as a weighted sum of a plurality of elements of the seventh data sequence with weighting controlled by values of second coefficients applied as input to the second filter.

16. The transceiver in accordance with claim 15

wherein the first means adjusts values of the first and second coefficients in response to edges of the first clock signal.

17. The transceiver in accordance with claim 16

wherein values to which the first means adjusts the first and second coefficients are functions of values of elements of the seventh data sequence.

18. The transceiver in accordance with claim 17 wherein the first means comprises:

a slicer (111) for rounding values of elements of the seventh data sequence to produce corresponding elements of an eight data sequence,

means (110-105) for generating a phase data value (D7) that is a function of a difference between corresponding elements of the seventh and eighth data sequences,

an accumulator (105) for accumulating the phase data value to produce a sequence of control data values (r) and for asserting a mask signal whenever the control data value reaches a predetermined limit;

means (106) responsive to the mask signal for masking edges of the first clock signal when the mask signal is asserted to produce the second clock signal;

means (100) for generating third clock signal in response to the first clock signal and the control data value such that the second frequency is a function of the control data value, and

means (84 and 96) for producing the first and second coefficients as functions of values of elements of the control data sequence.

19. The transceiver in accordance with claim 18 wherein the means (100) for generating third clock signal comprises:

means (101) responsive to the first clock signal for generating a plurality of reference clock signals, each having edges occurring with said first frequency but with each reference clock signal having a unique phase; and

means (103,104) for generating edges of the third clock signal in response to edges of the reference clock signals selected in accordance with values of the control data sequence.